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SEAT No.:	

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[5153] - 552 T.E. (E & TC)

DIGITAL SIGNAL PROCESSING

(2012 Pattern) (Semester - I) (End Sem.) (304182)

Time: 2½Hours] [Max. Marks:70

Instructions to the candidates:

- 1) Solve Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8, Q9 or Q10.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data if necessary.
- Q1) a) Draw the block diagram of Digital Signal Processing System and explain the Operation of each block, which additional component is needed to prevent aliasing.[4]
 - b) Consider the analog signal $X_a(t) = 3 \cos 2000\Pi t + 5 \sin 6000\Pi t + 10 \cos 12000\Pi t$ [6]
 - i) What is the Nyquist rate for this signal?
 - ii) If Sampling rate $F_s = 5000$ samples/s. What is the discrete time signal obtained after sampling?
 - iii) What is the analog signal $y_a(t)$ that we can reconstruct from the samples. If we use ideal interpolation?

OR

- **Q2)** a) Compute 4 point DFT of a sequence $x(n) = \{0,123\}$ using Decimation In Time FFT Algorithm. [5]
 - b) Compute the DFT of the following sequence $x(n) = \{1 \ 2 \ 3 \ 4\}$ and verify your answer using IDFT. [5]

P.T.O.

- (23) a) What is the relationship between Z transform and Fourier transform. [3]
 - b) Perform the circular convolution of the following sequence [4]

$$x_1(n) = \{ 1234 \}$$
 $x_2(n) = \{ 2121 \}$

c) By using partial fraction method find the Inverse Z transform of [3]

$$X(z) = \frac{z^3}{(z+1)(z-1)^2}$$
.

OR

- **Q4)** a) Show that the computational complexity is reduced if 32 point DFT is computed using Radix 2 DIT FFT algorithm. [3]
 - b) Compute the z transform and draw ROC of the following sequences[3]
 - i) $x(n) = n^2 u(n)$ for $n \ge 0$
 - ii) $x(n) = 2^{(n)}u(n-2)$
 - c) Compute the Discrete Cosine Transform of the following sequence [4] $f(x) = \{1 \text{ 2 4 7}\}$
- **Q5)** a) The system transfer function of an analog filter is given by [8]

$$H(S) = \frac{s + 0.1}{(s + 0.1)^2 + 9}$$

Using bilinear transformation method, determine the transfer function of digital filter H(z), the resonant frequency is $W_r = \frac{\pi}{4}$.

- b) Explain the steps used for designing an IIR filter using bilinear transformation method (BLT). What is Warping effect in BLT? [8]
- c) Describe Butterworth Filters? [2]

OR

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Q6) a) Obtain direct form I and II realization of a system described by $y(n) = b_1 x(n-1) + b_2 x(n-2) + b_3 x(n-3) - a_1 y(n-1) - a_2 y(n-2) - a_3 y(n-3)$

b) A digital filter has specifications as: [6]

Passband frequency= $W_p = 0.4\Pi$,

Stopband frequency = $W_s = 0.6\Pi$

What are the corresponding specifications for passband and stopband frequencies in analog domain if

- i) Impulse Invariance Technique is used for designing.
- ii) Bilinear Transformation Method is used for designing.
- c) Write a note on, "finite word length effect in IIR filter design". [4]
- Q7) a) Justify, FIR filters are linear phase filters. Define Phase delay and Group delay in linear phase filters.[8]
 - b) Design FIR digital filter to approximate an ideal low pass filter with passband gain of unity, cut off frequency 850 HZ and sampling frquency 5000 HZ. The length of impulse response should be 5. Use rectangular window. [8]

OR

- Q8) a) Compare the frequency domain characteristics of the different types of window Functions.[6]
 - b) A low pass filter is to be designed the following desired frequency response [10]

$$H_d(e^{jw}) = e^{-j2w} \quad \text{For } -\frac{\pi}{4} \le w \le \frac{\pi}{4}$$
$$= 0 \qquad \qquad \frac{\pi}{4} < |w| < \pi$$

Determine the filter coefficient $h_d(n)$ if the window function is defined as

$$w(n) = 1,$$
 $0 \le n \le 4$
= 0 otherwise

Also determine the frequency response H (e^{iw}) of the designed filter.

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Q9) a)	Design a two stage decimator for the following specifications:	[10]			
	Sampling rate of an input signal = 20 KHZ				
	Down sampler $D = 100$				
	Passband = 0 to 40 Hz				
	Transition band = 40 to 50 HZ				
	Passband ripple = 0.01				
	Stopband ripple = 0.002				
b)	Explain the application of DSP to voice processing.	[6]			
	OR				
Q10) a)	Draw and explain the architectural block diagram TMS 320C 67XX serion DSP Processor.				
b)	Explain the necessity of	[8]			
	i) MAC				
	ii) Barrel Shifter in Digital Signal Processors.				

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