Total No. of Questions : 6]

SEAT No. :

P41

[Total No. of Pages : 2

APR - 17/BE/Insem - 45

B.E. (Electrical)

VLSI DESIGN

(Elective - IV(d))

(2012 Pattern)

Time : 1 Hour] *[Maximum Marks : 30*

Instructions to the candidates:

1) ***Attempt Q. 1 or Q. 2, Q. 3 or Q. 4, Q. 5 or Q. 6***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate marks.***
4) ***Use of logarithmic tables, slide rules, Mollier Charts, electronic pocket calculator and steam tables is allowed.***
5) ***Assume suitable data if necessary.***

Q1) a) Write a short note on ALU. **[5]**

b) Explain RS flip-flop using NAND gate. **[5]**

OR

Q2) a) Differentiate between Moore and Mealy machine. **[5]**

b) Define Entity and architecture in VHDL. **[5]**

Q3) a) Explain data objects: constant and variable in VHDL. **[5]**

b) Explain the following statements used in VHDL with suitable examples: **[5]**

i) Process

ii) Case

OR

Q4) a) Explain structural type of modeling with an example. **[5]**

b) Write a VHDL code for 2:1 multiplexer using data flow modeling style. **[5]**

Q5) a) Define synthesizable statements in VHDL **[5]**

b) Differentiate between function and procedures in VHDL **[5]**

P.T.O

OR

Q6) a) Explain the term metastability with example. **[5]**

b) Write a short note on finite state machine. **[5]**

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