Tota	l No.	of Questions: 10] SEAT No.:	
P36	502	[Total N	o. of Pages : 2
		[4959]-1080A	
		B.E. (Electrical) (End Semester)	
		VLSI DESIGN	
		(2012 Pattern) (Elective - IV)	
Time	e: 2½	[Max	x. <i>Marks</i> : 70
	1) 2) 3) 4)	Attempt Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8, Q9 or Q10. Neat diagrams must be drawn wherever necessary. Figures to the right indicate full marks. Use of logarithmic tables, slide rules, Mollier Charts, electrological calculator and steam tables is allowed. Assume suitable data, if necessary.	tronic pocket
Q1)	a) b)		[6] machines in [4]
<i>Q</i> 2)	a)		Fevamnle [6]
<u> </u>	b)		
Q 3)	a)	Write VHDL code for 4-bit UP counter.	[6]
	b)	List the concurrent statements in VHDL.	[4]

OR Q4) a) Explain configurations in VHDL.

[6]

b) Draw a Moore FSM (state diagram) to detect sequence 1101. [4]

Q5) a) Differentiate CPLD w.r.t. FPGA

[8]

b) With neat schematic explain the architectural building blocks of FPGA.[8]

OR

P.T.O.

Q6)	a)	List the features, specifications and applications of FPGA.	[8]		
	b)	Explain the need of PLDs. Compare ASIC with DSP processor.	[8]		
<i>Q7</i>)	a)	Explain CMOS inverter and its transfer characteristics in detail.	[8]		
	b)	Draw and explain CMOS NAND and CMOS NOR gate	[8]		
		OR			
Q 8)	 a) Explain Static and dynamic power dissipation. Derive as power-delay product. 		for [8]		
	b)	Explain the following:i) Body effectii) Hot Electron Effect andiii) Velocity Saturation	[8]		
Q9)	a)		of 10]		
	b)	Differentiate between carry ripple adder and carry look ahead adder v diagram.	vith [8]		
	OR				
Q10)	a)	Explain with a FSM diagram a vending machine controller. [10]		
	b)	Explain barrel shifter with diagram.	[8]		



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