**NUMA** 

SEAT NO.	:	

[Total No. of Pages : 2]

## S.E. 2012 (Computer Engineering) Computer Organization (Semester -II)

Time: 2Hours Max. Marks: 50 Instructions to the candidates: 1) Answers Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8. 2) Neat diagrams must be drawn wherever necessary. 3) Figures to the right side indicate full marks. 4) Use of Calculator is allowed. 5) Assume Suitable data if necessary Q1) a) Using Booth's algorithm multiply the following [6] Multiplicand = 7, Multiplier = 3b) Explain IEEE 488 format for single precision and double precision floating point [6] numbers with example. OR Q2) Explain the various speeds up techniques of processor [4] a) Explain following addressing modes of 8086 with suitable examples [8] b) a. Index Addressing b. Register Indirect c. Auto Increment d. Relative Addressing Q3) Draw flowchart for Non restoring Division algorithm [6] a) Write control sequence for execution of the instruction [6] b) Add (R3), R1 OR Q4) Explain the Key components of the front end of the Intel Nehalem architecture. [6] a) What are the different design methods for Hardwired control units? Explain any [6] b) one. Q5) Explain cache mapping techniques with example [6] a) Explain Intel Nehalem memory organization with diagram b) [7] OR Write short Notes (Any Three) [13] Q6) **DDR3 Memory** 

## USB Packet Format PCI Bus

Q7)	a)	Draw and explain block diagram of itanium processor	
	b)	Write short note on	[7]
		1. i7 Mobile Version	
		2. Instruction format of IA-64 architecture	
		OR	
Q8)	a)	Explain the architecture of CBE processor with the help of block diagram	[6]
	b)	Write short note on	[7]
		1. Sun UltraSparc T1	
		2. NVIDIA GPU	