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[4957]-1080

S.E. (Comp. Engg.) (Second Year) EXAMINATION, 2016

COMPUTER ORGANIZATION

(2012 PATTERN)

Time : Two Hours

Maximum Marks : 50

1. (a) What are the different speed-up techniques for processor. [6]
- (b) Explain IAS computer with suitable diagram. [6]

Or

2. (a) Draw and explain function of E-flag and CR₀ of 80386. [6]
- (b) Explain IEEE standard single precision and double precision floating point formats. [6]
3. (a) Write micro-operations and control signals for ADD (R3), R1 instruction for single bus organization of CPU. [6]
- (b) Draw flow chart for restoring division operation. [6]

Or

4. (a) What are the advantages of pipelining ? Define latency and throughput of pipeline. [6]

P.T.O.

- (b) Compare hardwired control and microprogrammed control unit. [6]
5. (a) Explain with suitable diagram memory hierarchy in computer system. [6]
- (b) Explain the need of bus arbitration ? Explain daisy chaining scheme. [7]

Or

6. (a) Write a short note on DDR3 memory organization. [6]
- (b) Write a short note on Intel Nehalem memory organization with diagram. [7]
7. Write short notes on : [13]
- (i) Hyper-Transport Technology
- (ii) Instruction format of IA 64
- (iii) NVIDIA GPU architecture.

Or

8. (a) Write short notes on : [8]
- (i) Itanium processor
- (ii) Speculative Loading in IA64
- (b) Explain the technology supported and interfaces of i7 mobile version. [5]