

Total No. of Questions—8]

[Total No. of Printed Pages—3

Seat No.	
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[5668]-192

S.E. (Computer Engineering) (I Semester) EXAMINATION, 2019

MICROPROCESSOR ARCHITECTURE

(2012 PATTERN)

Time : Two Hours

Maximum Marks : 50

N.B. :— (i) Answer any *four* questions : Q. No. 1 or Q. No. 2,
Q. No. 3 or Q. No. 4, Q. No. 5 or Q. No. 6, Q. No. 7
or Q. No. 8.

(ii) Neat diagram must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Assume suitable data, if necessary.

1. (A) Define segment descriptor. [3]
(B) Describe in detail Memory Management Unit of 80386DX. [6]
(C) Describe call gate descriptor. [3]

Or

2. (A) Compare and contrast between 8086 with 80386 addressing
modes. [3]
(B) Describe in detail descriptor tables and descriptor with suitable
diagram representation. [6]
(C) Draw 8086 block diagram. [3]

P.T.O.

3. (A) Describe in detail privilege levels of 80386. [3]
(B) Explain in brief Linear to Physical address translation process of 80386. [5]
(C) Draw and explain Flag register of 80386. [4]

Or

4. (A) Draw and explain complete bus cycle state diagram. [3]
(B) Describe in detail of control, Test and Debug register of 80386. [5]
(C) Contrast between POP, POPA, POPAD. [4]
5. (A) Define Multicore. List types of Multicore architectures. [3]
(B) What do you as a designer and developer of software need to know about moving from sequential programming and single core application development to multicore programming ? [6]
(C) What are differences between dual and quad core CMP. [4]

Or

6. (A) Enlist features of parallel programming with diagram. [3]
(B) Describe with block diagram of 'The BUS' connection. [6]
(C) Write in brief hyper-threading CMP. [4]

7. (A) Explain entering and leaving VM 86 mode in detail. [3]
(B) Draw and explain block diagram of 64-bit architecture. [6]
(C) Write a short note on virtualization technology. [4]

Or

8. (A) Describe in detail Intel Microarchitecture code name Nehalem. [3]
(B) Explain in detail registers in IA 32 architecture. [6]
(C) Write a short note on SIMD instruction. [4]