Total No of Questions: [8] *SEAT NO. :*

[Total No. of Pages : *1*]

S.E. 2012 (Electronics/E&Tc)

COMPUTER ORGANIZATION

(Semester - II)

Time: 2 Hours ***Max. Marks : 50***

Instructions to the candidates:

1) ***Neat diagrams must be drawn wherever necessary.***
2) ***Figures to the right side indicate full marks.***
3) ***Assume Suitable data if necessary***

Q1)	a)	Draw and explain the Von Neumann architecture	[6]
	b)	Represent $(178.1875)_{10}$ in single precision floating point format	[6]
		OR	
Q2)	a)	Explain pipelining & superscalar operation	[6]
	b)	multiply the following numbers using bit pair recoding method Multiplicand 01111 (15) Multiplier 10110 (-10)	[6]
Q3)	a)	Write control sequence for execution of instruction ADD (R1), R2 using single bus organization	[6]
	b)	Draw and explain the interface between printer and processor	[6]
		OR	
Q4)	a)	Explain different methods to handle multiple interrupt requests	[6]
	b)	Explain the steps involved in fetching a word from memory	[6]
Q5)	a)	Draw and explain the structure of Asynchronous DRAM and hence explain how the data can be read or written in the DRAM	[7]
	b)	Explain different mapping schemes for cache memory	[6]
		OR	
Q6)	a)	Explain the concept of virtual memory.Explain how virtual address is translated to physical address.	[6]
	b)	With the help of a neat diagram, explain the working principle of SRAM	[7]
Q7)	a)	Explain the following instructions of 8086 with suitable example i) XLAT ii)DAA iii) PUSH iv) IN v) TEST vi) LEA	[6]
	b)	Explain interrupt structure of 8086	[7]
		OR	
Q8)	a)	Explain the following addressing modes of 8086 with examples i) String addressing ii) Based Indexed addressing iii) Direct addressing	[6]
	b)	Draw the bit pattern for flag register of 8086 and explain significance of each bit	[7]