Total No. of Questions—8] [Total No. of Printed Pages—2

| Seat No. | |
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# [5352]-139

## S.E. (E&TC/Elect.) (Second Semester) EXAMINATION, 2018

## COMPUTER ORGANIZATION

## (2012 PATTERN)

**Time : Two Hours** **Maximum Marks : 50**

***N.B.*** :— (*i*) Neat diagrams must be drawn wherever necessary.

(*ii*) Figures to the right indicate full marks.

(*iii*) Use of logarithmic tables slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.

(*iv*) Assume suitable data if necessary.

**1.** (*a*) Draw and explain the Von-Neumann Architecture. [6]

(*b*) Multiply (-7) and (3) using Booths algorithm. Register size 5 bits. [6]

*Or*

**2.** (*a*) Draw and explain multiple bus organization of CPU. [6]

(*b*) Represent $(178.1875)_{10}$ in single and double precision floating point format. [6]

**3.** (*a*) Represent (–13) in Booths recoded format and bit-pair recoded format. [6]

(*b*) Differentiate between hardwired and micro-programmed control. [6]

P.T.O.

*Or*

**4.** (*a*) Explain different methods to handle multiple interrupt request. [6]

(*b*) Explain any *two* DMA data transfer modes. [6]

**5.** (*a*) Write a short note on Virtual memory. [6]

(*b*) Explain different mapping schemes for cache memory. [7]

*Or*

**6.** (*a*) Write short note on Synchronous DRAM. [6]

(*b*) Explain the connection of memory to processor. [7]

**7.** (*a*) Explain functions of the following pins of 8086 : [6]

(*i*) NMI

(*ii*) INTR

(*iii*) RESET.

(*b*) Draw the bit pattern for flag register of 8086 and explain significance of each bit. [7]

*Or*

**8.** (*a*) List out the features of 8086. [6]

(*b*) Explain logical to physical addressing of 8086. [7]