SEAT No.	:	

P3603

[Total No. of Pages: 2

## [4959] - 1081

		BE (E & TC)	
		VLSI Design & Technology (End - Sem)	
		(2012 Pattern)	
Time :2½ Hours] [Ma		[Max. Marks:	70
Instr	uctio	ons to the candidates:-	
	<i>1</i> )	Neat diagrams must be drawn wherever necessary.	
	<i>2</i> )	Use of electronic pocket calculator is allowed.	
	<i>3</i> )	Assume suitable data, if necessary.	
	<i>4</i> )	Answer any one questions out of Q.1 or Q.2, Q.3 or Q.4, Q5 or Q6, Q.7 or Q	.8.
<b>Q</b> 1)	a)	What is meant by concurrent & sequential statements in VHDL? Exploin detail with two examples of each.	ore [ <b>7</b> ]
	b)	With the help of suitable schematics, compare PROM, PLA & PA architectures. What is need of CPLD?	\L [7]
	c)	What is clock skew? Explain the solutions to it.	[6]
		OR	
<b>Q</b> 2)	a)	Write VHDL code for Mod - N counter. Write suitable test bench for it.[	[7]
	b)	Explain PLD targeted design flow in detail.	[7]
	c)	What is supply & ground bounce? What are remedies to it?	[6]
Q3)	a)	Draw ac equivalent ckt of MOSFET & explain various capacitance involved.	es [ <b>9</b> ]
	b)	What is technology scaling? What are types? Explain each in detail. [	9]
		OR	
<b>Q4</b> )	a)	With the help of mathematical analysis & suitable schematic, explain E transfer characteristics of CMOS Inverter.	OC [ <b>9</b> ]
	b)	What are merits of transmission gate? Design 4: 1 mux using transmission gates.	on [ <b>9</b> ]

*P.T.O.* 

<b>Q</b> 5)	a)	Draw the ckt diagram for push pull CMOS inverter as an amplifier explain. Give the expressions for output voltage range, output resistant & bandwidth.	
	b)	With the help of suitable schematic, explain cascode amplifier. What its merits? Give the expressions for voltage gain and output resistance.	
		OR	
<b>Q6</b> )	a)	Explain current mirror in detail. Why is it needed?	[8]
	b)	Explain current sink & current source in detail. Give expressions output voltage range & output resistance.	for [ <b>8</b> ]
<b>Q7</b> )	a)	What are the types of fault? Explain each in brief.	[8]
	b)	What is need of BIST? Explain typical BIST in detail.	[8]
		OR	
<b>Q</b> 8)	a)	With the help of block diagram, explain TAP controller in detail.	[8]
	b)	Explain boundary scan technique.	[8]

