Total No. of Questions : 8]

SEAT No. :

P3111

[Total No. of Pages : 2

[5354]-601
B.E. (Semester - I)
ELECTRONICS & TELECOMMUNICATION
VLSI Design & Technology
(2012 Pattern)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates :

1) ***Answer any one question out of Q.No.1 or 2, Q.No.3 or 4, Q. No. 5 or 6, Q.No.7 or 8.***
2) ***Neat diagrams should be drawn wherever necessary.***
3) ***Use of electronic pocket calculator is allowed.***
4) ***Assume suitable data, if necessary.***

Q1) a) Write VHDL code for 1011 Moore sequence detector with test bench. **[8]**

b) What are the limitations of PLD Architectures? **[6]**

c) Explain Interconnect Routing Techniques. **[6]**

OR

Q2) a) What are attributes? Explain various types of attributes used in VHDL. **[8]**

b) Draw and explain the detail architecture of FPGA. **[6]**

c) Write short note on I/O Architecture. **[6]**

Q3) a) Explain the static and dynamic power dissipation. **[4]**

b) Explain power delay product and state its significance. **[4]**

c) Design CMOS logic for Y=ABC+D. Calculate W/L ratio for N_{mos} and P_{mos} area needed on chip. **[10]**

P.T.O.

OR

Q4) a) Explain CMOS inverter and its transfer characteristics in detail. How to achieve Symmetry in the characteristics. **[8]**

b) Draw NAND, NOR. AND, OR, EX-OR gates using CMOS. **[10]**

Q5) a) Explain MOS device as resistor and diode, with the help of equivalent diagram. **[8]**

b) Draw and explain of CMOS difference amplifier circuit? **[8]**

OR

Q6) a) Draw and explain push pull CMOS inverter .Also draw its small signal model. **[8]**

b) Write short note on cascade amplifier. **[8]**

Q7) a) Explain controllability and observability. **[8]**

b) What is JTAG? List the different signals involved. **[8]**

OR

Q8) a) Compare Testability and Verification. **[8]**

b) Explain Built In Self Test (BIST). **[8]**

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