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B.E. (E&TC)

VLSI DESIGN & TECHNOLOGY

(2012 Pattern) (Semester - I) (404181)

Time : 2½ Hours]   *[Max. Marks : 70*

Instructions to the candidates:

   1)   *Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.*

   2)   *Assume suitable data if necessary.*

Q1) a)   Explain the behavioral, data flow, structural VHDL modeling techniques with example. What are the relevant advantages of each?   **[8]**

     b)   Draw and explain the block diagram CPLD architecture.   **[6]**

     c)   Explain power distribution and power optimization techniques.   **[6]**

OR

Q2) a)   Draw the state diagram of lift controller for two floors. Write optimum VHDL code for it.   **[8]**

     b)   Explain the following terms.   **[6]**

        i)   CLB

        ii)   UCF

        iii)   GRM

        iv)   EDIF

     c)   What are the wires parasitic? How it effect the performance in the VLSI chip Design?   **[6]**

Q3) a)   Explain in detail static and Dynamic power dissipation.   **[8]**

     b)   With the help of mathematical analysis & suitable schematic, explain DC transfer Characteristics of CMOS Inverter.   **[10]**

OR

P.T.O.

Q4) a) Design CMOS logic for Y = AB+CDEFG+H. **[10]**

b) Explain the following terms: **[8]**

i) Body effect

ii) Hot Electron effect

iii) Velocity saturation

iv) Power delay product

Q5) a) Compare push-pull, current source & active load inverters with respect to voltage gain, voltage range, output resistance & bandwidth in detail.**[8]**

b) With the help of suitable schematic, explain cascode amplifier. What are its merits? Give the expressions for voltage gain and output resistance.**[8]**

OR

Q6) a) Draw schematic diagram and I-V characteristics, explain current sink and current source. **[8]**

b) Draw common drain amplifier. Compare with common source & common gate amplifiers with respect to gain, output resistance & bandwidth. **[8]**

Q7) a) Draw and explain JTAG in detail. **[8]**

b) Explain in detail boundary scan technique. **[8]**

OR

Q8) a) Explain: **[8]**

i) Partial scan and full scan

ii) Stuck at '1' and '0' faults

b) Write short note on BIST. **[8]**

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