Total No. of Questions : 6]

SEAT No. :

P4875

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B.E./Insem. - 38

B.E. (E & T/C)

VLSI DESIGN & TECHNOLOGY

(2012 Pattern) (Semester - I)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates:

1) ***Answer Q1 or Q2, Q3 or Q4, Q5 or Q6.***
2) ***Figures to the right side indicate full marks.***

Q1) a) Explain different architectural modeling types in VHDL. Give brief example of each. **[5]**

b) Write VHDL code for 4 : 1 MUX & write test bench for it. **[5]**

OR

Q2) a) Draw FSM diagram & write VHDL code for 100 Moore sequence detector. **[5]**

b) What is need of function? Explain function call & function body in brief. **[5]**

Q3) a) Explore the architecture of FPGA in detail. **[5]**

b) Compare CPLD w.r.t FPGA. **[5]**

OR

Q4) a) How does logic get implement in CPLD & FPGA? What is conceptual difference? **[5]**

b) Explore Place & Rout (PAR) as well as timing verification w.r.t. CPLD/ FPGA. **[5]**

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Q5) a) List & explain signal integrity issues. **[5]**

b) What is need of power optimization? Explain any one method. **[5]**

OR

Q6) a) What is clock jitter? How to eliminate? **[5]**

b) Explore interconnect routing techniques. **[5]**

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