Total No. of Questions : 6]

SEAT No. :

P81

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OCT. -16/BE/Insem. - 136
B.E. (E & TC)
VLSI DESIGN & TECHNOLOGY
(2012 Course)

Time : 1Hour] *[Max. Marks :30*

Instructions to the candidates:

1) ***Solve Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q6.***
2) ***Figures to the right side indicate full marks.***

Q1) a) What is meant by synthesizable & non-synthesizable statement? Give two examples of each. **[5]**

b) Write VHDL code for half adder by structural & behavioural modeling. **[5]**

OR

Q2) a) List & explain different delays involved in chip design. **[5]**

b) Explain data objects with suitable examples. **[5]**

Q3) a) Compare PROM, PLA, PAL & CPLD. **[5]**

b) Explore CPLD/FPGA oriented design flow. **[5]**

OR

Q4) a) Draw CPLD architecture in detail. Explain in brief. **[5]**

b) Give typical features & specifications of FPGA. **[5]**

Q5) a) What is clock skew? What are techniques to minimize? **[5]**

b) Why should supply & ground bounce be taken care? How are these minimized? **[5]**

OR

Q6) a) Explore different wire parasitics. **[5]**

b) With the help of suitable diagram, explain I/O architecture in brief. **[5]**