Total No. of Questions : 8]

SEAT No. :

P3653

[Total No. of Pages : 2

[4859]-1036

B.E. (E & T/C)

VLSI DESIGN & TECHNOLOGY

(2012 Pattern) (Semester - I)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Answer any one question out of Q.No.1 or 2, Q.No.3 or 4, Q.No. 5 or 6, Q.No.7 or 8.***
2) ***Neat diagrams should be drawn wherever necessary.***
3) ***Use of electronic pocket calculator is allowed.***
4) ***Assume suitable data, if necessary.***

Q1) a) Write VHDL code for 8 bit serial in serial out shift register by structural & behavioural modeling methods. **[7]**

b) What is need of FPGA? List typical specifications of FPGA. **[7]**

c) Explain I/O architecture in detail. **[6]**

OR

Q2) a) What are flip flop timings? What is meta-stability? What are solutions? **[7]**

b) Explore the architecture of CPLD in detail. **[7]**

c) What are different wire parasitics? How do they play important role in routing? **[6]**

Q3) a) Derive the expressions for power dissipations in CMOS. What are the techniques to minimize the dissipations? **[9]**

b) Design CMOS logic for Y = AB + CDEFG+H. Compute area on chip. **[9]**

OR

Q4) a) What is power delay product? Derive the expression for it. What is its significance? **[9]**

b) Explain linear delay model in detail. **[9]**

P.T.O.

Q5) a) Compare push-pull, current source & active load inverters with respect to voltage gain, voltage range, output resistance & bandwidth in detail. **[8]**

b) Draw the schematic of CMOS differential amplifier and give the expressions for voltage gain, output resistance. CMRR & ICMR. **[8]**

OR

Q6) a) Draw common drain amplifier. Compare with common source & common gate amplifiers with respect to gain, output resistance & bandwidth. **[8]**

b) Draw & explain CMOS operational amplifier. Give the expressions for voltage gain & output resistance. **[8]**

Q7) a) What is need of DFT? Explain with suitable example. **[8]**

b) Explain fault models in detail. **[8]**

OR

Q8) a) With the interface ports involved, explain JTAG in detail. **[8]**

b) What is partial & full scan path? **[8]**