

Total No. of Questions : 8]

SEAT No. :

P2264

[Total No. of Pages : 2

[5254]-601

**B.E. (Electronics & Telecommunication)**

**VLSI DESIGN & TECHNOLOGY**

**(2012 Pattern) (Semester - I)**

*Time : 2½ Hours]*

*[Max. Marks : 70*

*Instructions to the candidates:*

- 1) *Answer Q. 1 or Q. 2, Q. 3 or Q. 4, Q. No. 5 or Q. 6 and Q.7 or Q. 8.*
- 2) *Neat diagrams should be drawn wherever necessary.*
- 3) *Use of electronic pocket calculator is allowed.*
- 4) *Assume Suitable data if necessary.*

- Q1)** a) Explain Metastability with timing diagram. [6]  
b) Draw and explain the detail architecture of CPLD. [8]  
c) Explain positive and negative clock skew. Briefly explain the sources of clock skew. [6]

OR

- Q2)** a) Write VHDL code and test bench for 1011 Mealy sequence detector. [8]  
b) What factors are considered to make a choice in between FPGA and CPLD? [6]  
c) Outline power distribution and optimization. [6]

- Q3)** a) Which lambda rules are used for CMOS layout? Give its significance. [8]  
b) Design CMOS logic for  $YA = \overline{A(D + E) + BC}$ . Calculate W/L ratio for  $N_{MOS}$  and  $P_{MOS}$  area needed on chip. [10]

OR

- Q4)** a) Explain the static and dynamic power dissipation. [6]  
b) What is technology scaling? What are its effects? [6]  
c) Draw and Explain the RC Delay Model for nMOS and pMOS transistor. Give example. [6]

*P.T.O.*

- Q5)** a) Explain various types CMOS inverting amplifier with diagram. [8]  
b) Explain small signal low frequency and small signal high frequency model of MOS transistor with diagram. [8]

OR

- Q6)** a) Draw and explain CMOS operational amplifier. [8]  
b) Draw and explain current mirror circuits. [8]

- Q7)** a) Describe types of faults? Explain with schematic. [8]  
b) Explain JTAG boundary scan. Which are the various pins involved. [8]

OR

- Q8)** a) Draw and explain the architecture of TAP Controller. [8]  
b) What is scan path? Give advantages and disadvantages of scan path. [8]

