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BOARD DIPLOMA EXAMINATION, (C–09)
MARCH/APRIL—2018
DCE—THIRD SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours]   [*Total Marks* : 80

PART—A   3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Add the following binary numbers :

(a) 1011_2 and 1110_2

(b) 1101_2 and 110_2

(c) 10111_2 and 11_2

2. Divide the binary number 1100_2 by 100_2.

3. Define 'fan-in', 'fan-out' and 'power dissipation' of logic families.

4. Draw a one-bit digital comparator.

5. What is a multiplexer?

6. What are sequential logic circuits?

7. Draw a level clocked T flip-flop.

8. List three IC numbers for registers.

9. Draw the circuit of A/D converter using counter method.

10. List any three RAM ICs.

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PART—B   10×5=50

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Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. Draw the logic circuits for the realization of AND, OR and NOT operations using NAND and NOR gates.

12. *(a)* Draw the sum of products circuit for the following equation :   5

$$Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,B\,\overline{C}$$

(b) Write the Boolean expressions of sum of minterms from the following truth table and simplify :   5

	Input		Output
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

13. Draw and explain the BCD to decimal decoder.

14. Draw and explain the logic circuit of a full-adder. Derive the expressions for both carry and sum.

15. Draw and explain *R-S* flip-flop along with truth table using NAND gates.

16. With a neat diagram, explain the operation of shift left register.

17. *(a)* Explain the terms 'resolution', 'accuracy' and 'monotonicity' of converter.   5

    (b) Draw *R-2R* ladder network D/A converter.   5

18. *(a)* State memory read operation write operation.   5

    (b) Define access time, memory capacity and word length.   5

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