

## 4240

## **BOARD DIPLOMA EXAMINATION, (C-14)**

MARCH / APRIL - 2019

## DECE - III SEMESTER EXAMINATION DIGITAL ELECTRONICS

Time: 3 Hours [Total Marks: 80

## PART - A

 $3 \times 10 = 30$ 

Instructions:

- (1) Answer ALL questions.
- (2) Each question carries **THREE** marks.
- (3) Answer should be brief and straight to the point and shall not exceed five simple sentences.
- 1 State De-Morgan's Theorems.
- 2 Draw the symbols of universal logic gates with Truth Tables.
- 3 Convert the hexadecimal number (AB6.13) into equivalent octal number.
- 4 List the important characteristics of digital IC's.
- 5 Draw the Half-adder circuit with NAND gates and give output functions.
- 6 List any 3 applications of multiplexer circuit.
- 7 Define Race around Condition.
- 8 State the need for a Register.
- 9 List any 3 applications of shift registers.
- 10 Write the differences between ROM and RAM.

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		PART - B 10×5=5	50
Insti	ructio	(1) Answer any FIVE questions. (2) Each question carries TEN marks. (3) Answer should be comprehensive and the criteric for valuation is the content but not the length the answer.	
11	(a)	Write the difference between weighted codes and	4
		Un-weighted codes.	
	(b)	(i) Subtract 1101 from 1000 using 2's complement method.	2
		(ii) Convert 87 to Excess-3 code.	2
		(iii) Convert (1001101) <sub>2</sub> into gray code.	2
12	(a)	Develop the basic gates AND, OR NOT using NAND	6
		and NOR gates.	
	(b)	•	4
	` ′	$Y = \overline{ABC} + A\overline{BC} + \overline{ABC} + ABC + \overline{ABC}$	
13		ain the working of open collector TTL NAND gate with reuit diagram.	
14	(a)	Explain 2's complement parallel adder/subtractor circuit.	6
	(b)	Comparison between serial adder and parallel adder.	4
15	Expl	ain the working of BCD to Decimal decoder circuit.	
16		w and explain the working of clocked SR flip-flop using ND gates with Truth Table.	
17	Explain the working of (a) 4 bit shift left register (b) 4-bit shift right register with circuit diagrams.		
18	-	ain the working of 4-bit asynchronous counter with a circuit timing diagram.	

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