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C14–EC–606

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BOARD DIPLOMA EXAMINATION, (C–14)

MARCH/APRIL—2018

DECE—SIXTH SEMESTER EXAMINATION

DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.
(2) Each question carries **three** marks.
(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. What are the advantages of CMOS technology?

2. List the features of verilog HDL.

3. Identify the components of verilog module definition.

4. Write about 'initial' and 'always' statements.

5. What are the types of conditional statements?

6. Write verilog code for 4 : 1 multiplexer.

7. Compare between RTL level and structural level modelling.

8. Define test bench module.

9. What are different types of finite statement machine? Define them.

10. List the programmable logic devices.

PART—B

10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. Explain the VLSI design flow.

12. Explain about *(a)* ports, *(b)* identifiers, *(c)* key words and *(d)* system tasks.

13. Explain about four 'looping' statements.

14. Design a 8 to 3 encoder circuit using verilog coding.

15. Design a *D* flip-flop with asynchronous reset using verilog coding.

16. Write the test bench for 4 : 1 multiplexer using verilog coding.

17. *(a)* Explain the concept of FSM.

(b) Explain about Moore state machine with one example.

18. Explain the architecture of PALs.

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