C14-EC-606

4742

BOARD DIPLOMA EXAMINATION, (C-14)

MARCH / APRIL - 2019

DECE - VI SEMESTER EXAMINATION

DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL

Time : **3** Hours] [Total Marks : **80**

PART - A **3×10=30**

Instructions : *(1) Answer **ALL** questions.*
*(2) Each question carries **THREE** marks.*
(3) Answer should be brief and straight to the point and shall not exceed five simple sentences.

1 List the advantages of CMOS technology.

2 Compare VHDL and Verilog HDL.

3 Define expressions, operators and operands.

4 Define rise, fall and turn-off delays in gate level design.

5 List the advantages of hierarchical modeling.

6 Write the Verilog code for Half-adder using data flow level modeling.

7 Write any three differences between RTL level and Structural modeling.

8 Define test bench module.

9 State the need for stimulus module.

10 List the programmable logic devices.

PART - B 10×5=50

Instructions : *(1) Answer any **FIVE** questions.*
*(2) Each question carries **TEN** marks.*
(3) Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11 Explain : **5+5**

(a) Design specification and Design entry

(b) Planning placement and Routing.

12 Explain the following Lexical conventions :

(a) Number specifications

(b) Identifiers

(c) Keywords

13 Explain Blocking and Non-blocking procedural Assignments with examples.

14 Design a divide by 3 counter using behavioural modeling in verilog.

15 Design verilog modeling of SIPO shift register using gate level modeling.

16 Explain :

(a) The concept of Finite State machine. **4**

(b) Moore machines and mealey machines. **6**

17 (a) Write the test bench code for JK flip flop. **5**

(b) Write the test bench code for Full-adder. **5**

18 Explain the architecture of FPGA. And give its applications. **7+3**
