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C14-EC-606

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BOARD DIPLOMA EXAMINATION, (C-14)
OCTOBER/NOVEMBER-2018
DECE-SIXTH SEMESTER EXAMINATION

DIGITAL CIRCUIT DESIGN THROUGH VERILOG HDL

Time : 3 Hours] [Total Marks: 80

PART-A

3X10=30

Instructions :

1. Answer **All** questions.
2. Each question carries **Three** marks.
3. Answer should be brief and straight to the point and shall not exceed five simple sentences.

1. What are the advantages of CMOS technology?
2. Compare VHDL and Verilog HDL?
3. Wrote the use of defparam and localparam keywords.
4. Define Rise time delay, Fall time delay and Turn-off delay in the gate level design.
5. List the conditional statements with syntax.
6. Write a behavioral modeling for D-Flip flop.
7. Compare RTL and structural modeling.
8. Define test-bench module.
9. Write the test bench for 4-to-1 multiplexer.
10. Compare PAL and PLA

PART-B

10X5=50

Instructions :

1. Answer any **Five** questions, choosing at least one from each section.
2. Each question carries **ten** marks.
3. Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer

11. Explain the nMOS fabrication steps with neat diagram.

12. Explain the lexical conventions

    (a) White space (b) Comments (c) Strings (d) Identifiers and Keywords

13. Explain the initial and always statements with examples.

14. Design a JK flip flop logic circuit and write verilog code.

15. Design the serial in serial out (SISO) shift register and write verilog code.

16. Explain the structure of stimulus module.

17. Explain the Melay type of state machines with examples.

18. Explain the architecture of FPGAs.

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