C14-EE-505

4637

BOARD DIPLOMA EXAMINATION, (C-14)

MARCH / APRIL - 2019

DEEE - V SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : **3** Hours]   [Total Marks : **80**

PART - A   **3×10=30**

Instructions :   (1) Answer **ALL** questions.
                       (2) Each question carries **THREE** marks.
                       (3) Answer should be brief and straight to the point
                            and shall not exceed five simple sentences.

1   Convert $736.65_{(8)}$ octal number in to binary number system.

2   State and explain de-Morgan's theorems.

3   Define the terms : (i) fan-in   (ii) fan-out.

4   Draw the diagram of TTL NAND gate with totempole output.

5   Draw the logic circuit of half adder using EX-OR and AND gates,
          give its truth table.

6   State the need for tri-state buffer, draw its symbol.

7   Compare TTL, CMOS, ECL logic families.

8   Explain NOR latch with truth table.

9   What is race around condition ?

10   Distinguish between NVRAM and flash ROM.

PART - B   10×5=50

Instructions :   (1) *Answer any **FIVE** questions.*

(2) *Each question carries **TEN** marks.*

(3) *Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer.*

11   Draw the NOT, AND, OR gates using NAND, NOR gates only.   **10**

12   Draw and explain TTL NAND gate open collector type circuit.   **10**

13   (a)   Define (i) propagation delay (ii) power dissipation   **3×2**
(iii) noise margin.

(b)   Draw the circuit of CMOS NAND gate circuit.   **4**

14   Draw and explain 4-bit parallel adder circuit.   **10**

15   (a)   Draw and explain 4×2 encoder circuit.   **7**

(b)   Draw the circuit of 2×4 decoder circuit.   **3**

16   Explain the operation of master – slave JK flip flop with neat   **10**
diagram.

17   Explain the operation and decade counter.   **10**

18   Explain a simple diode ROM.   **10**

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