## 4637

# BOARD DIPLOMA EXAMINATION, (C-14) <br> OCTOBER/NOVEMBER-2018 <br> DEEE-FIFTH SEMESTER EXAMINATION 

## DIGITAL ELECTRONICS

Time : 3 Hours ]
[ Total Marks: 80

## PART-A

$$
3 \times 10=30
$$

Instructions : 1. Answer All questions.
2. Each question carries Three marks.
3. Answer should be brief and straight to the point and shall not exceed five simple sentences.

1. What is even parity and what is odd parity.
2. Convert binary number 10010 into Gray code.
3. Define the term Propagation Delay and Fan-Out.
4. Write any three comparison between TTL and ECL logic family,
5. Give the IC numbers of following gates
a. 2-Input -AND gate
b. 2-Input -OR gate
c. 2-Input -NAND gate
6. State the need for Tri-State Buffer.
7. Draw the half adder circuit and write its truth Table.
8. List any three applications of Flip-Flops.
9. What is Race-Around condition?
10. Write any three differences between ROM and RAM

## PART-B

## Instructions : 1. Answer any Five questions.

2. Each question carries ten marks.
3. Answer should be comprehensive and the criterion for valuation is the content but not the length of the answer
4. Realize AND, OR, NOT operations by using NAND and NOR Gates.
5. Draw and Explain TTL NAND gate with Open Collector.
6. Draw and Explain the basic Emitter Coupled logic OR/NOR Gate.
7. (a) Draw and explain the operation of $4 \times 1$ Multiplexer.
(b) Draw the Full Adder circuit and verify its functionality using Truth Table.
8. Draw and explain Decimal to BCD Encoder.
9. Explain SR Flip-Flop using NAND and NOR Latches.
10. Explain Circuit of Level Clocked JK Flip-Flop with Truth table.
11. Explain the working of Dynamic MOS RAM cell and Static MOS Ram Cell.
